QSFP-DD 400Gb/s 1310nm 10km LR4 Transeivers

TD13C4L-CP Product Specification

FEATURES

- Up to 106.25Gb/s (PAM4) data rate per channel
- QSFP-DD MSA Compliant
- Duplex LC connector
- Maximum 10km link length over single-mode fiber
- CWDM4 EML /PIN
- Low Power Dissipation, Max 10W
- Operating Case Temperature: 0℃~70℃
- CMIS Compliant
- 400G-LR4-10 Technical Specification Compliant
- RoHS Compliant

APPLICATIONS

- 400GBASE-LR4-10 Ethernet
- Switch & Router Connections
- Data Centers
- Other 400G Interconnect Requirements

ORDERING INFORMATION

Part Number	From Factor	Data Rate	Media	Distance (km)	Wavelength	Temperature (℃)
TD13C4L-CP	QSFP-DD	425Gb/s	SMF	10	CWDM4	0~70

GENERAL PRODUCT CHARACTERISTICS

Parameter	Value	Unit	Comments
Module Form Factor	QSFP-DD		
Maximum Aggregate Data Rate	425	Gb/s	
Protocols Supported	400GE		
Electrical Interface and Pin-out	76-pin edge connector		Per QSFP-DD MSA
Maximum Power Consumption	10	Watts	
Management Interface	Serial, I2C-based, 400 kHz maximum frequency		Per QSFP-DD MSA

1. ABSOLUTE MAXIMUM RATINGS

Exceeding the limits below may damage the transceiver permanently.

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Note
Maximum Supply Voltage	V_{cc}	0		3.6	V	
Storage Temperature	T_{sto}	-40		85	℃	
Relative Humidity (Non-condensing)	RH	5		95	%	

2.RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Note
Supply Voltage	V_{cc}	3.135	3.3	3.465	V	
Case Operating Temperature	T_{op}	0		70	℃	
Relative Humidity (Non-condensing)	RH	15		85	%	
I2C clock frequency			100	400	kHz	
Pre-FEC Bit Error Ratio				2.4E-4		
Post-FEC Bit Error Ratio				1.0E-12		1
Link Distance		0.002		10	km	1,2

Notes:

1. FEC is provided by host system.
2. FEC is required on host system to support maximum distance.

3.ELECTRICAL CHARACTERISTICS

Parameter	Unit	Min.	Typ.	Max.	TP[1]	Note
Transmitter						
Signaling Rate	GBd	26.5625±100ppm			TP1	
Differential Data Input Voltage Peak to Peak Swing	mVpp	900			TP1a	2
Differential Input Return Loss	dB	Equation (83E-5)			TP1	
Differential to Common Mode Input Return Loss	dB	Equation (83E-6)			TP1	
Differential Termination Mismatch	%			10	TP1	
Module Stressed Input Test		See 120E.3.4.1			TP1a	3
Single-ended Voltage Tolerance Range	V	-0.4		3.3	TP1a	
DC common mode voltage	mV	-350		2850	TP1	4
Differential Input Impedance	Ohm	90		110	TP1	
Receiver						
Signaling Rate	GBd	26.5625±100ppm			TP4	
Differential Data Output Voltage Peak to Peak Swing	mV			900	TP4	
AC common mode voltage(RMS)	mV			17.5	TP4	
Transition Time, 20% to 80%	ps	9.5			TP4	
Differential Output Return Loss	dB	Equation (83E-2)			TP4	
Common to Differential Mode Conversion	dB	Equation (83E-3)			TP4	
Differential Termination Mismatch	%			10	TP4	
DC common mode voltage	mV	-350		2850	TP4	4
Differential Output Impedance	Ohm	90		110	TP4	

Notes

1. The location of TP1, TP1a and TP4 are defined in IEEE 802.3bs Figure 120E-5 and Figure 120E-6.
2. With the exception to IEEE 802.3bs 120E.3.1.2 that the pattern is PRBS31Q or scrambled idle.
3. Meets BER specified in IEEE 802.3bs 120E.1.1.
4. DC common mode voltage generated by the host. Its specification includes effects of ground offset voltage.

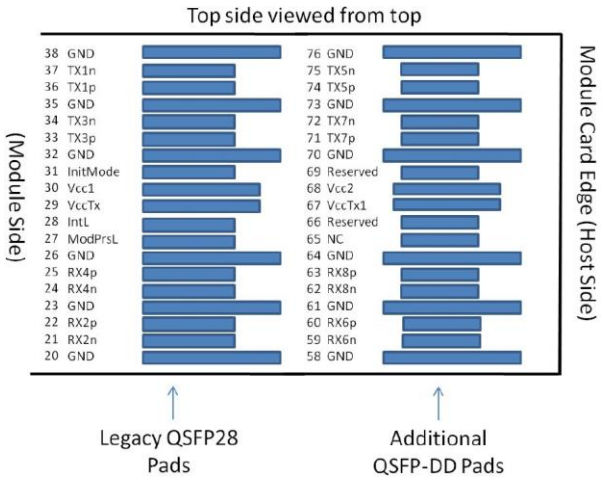
4.OPTICAL CHARACTERISTICS

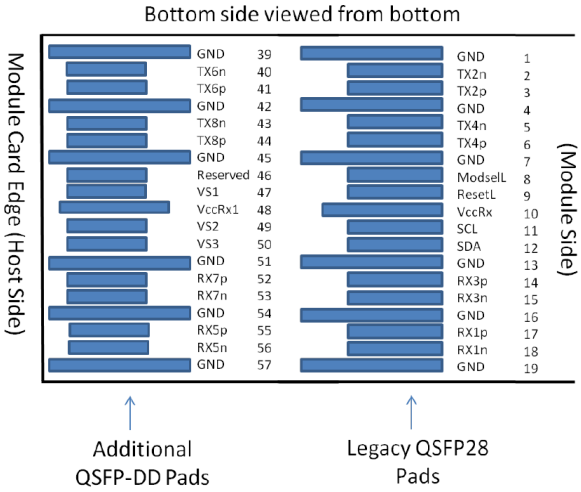
Parameter	Symbol	Min.	Typ.	Max.	Unit.	Note
Transmitter						
Signaling Rate			53.125±100ppm		GBd	1
Modulation format			PAM4		-	
Optical central wavelength	λ0	1264.5	1271	1277.5	nm	
	λ1	1284.5	1291	1297.5	nm	
	λ2	1304.5	1311	1317.5	nm	
	λ3	1324.5	1331	1337.5	nm	
Side Mode Suppression Ratio	SMSR	30	-	-	dB	
Total average launch power				11.1	dBm	
Average launch power	P_{avg}	-2.8		4	dBm	1,2
Outer Optical Modulation Amplitude	OMA_{outer}	0.3		3.7	dBm	3
		−1.1 + TDECQ		3.7	dBm	4
Difference in launch power between any two lanes (OMA_{outer})				4	dB	
Extinction Ratio	ER	3.5			dB	1
Average Launch Power with TX_OFF	P_{OFF}			-20	dBm	1
Transmitter and dispersion eye closure for PAM4	TDECQ			3.9	dB	1
Transmitter reflectance				-26	dB	
Receiver						
Signaling Rate			53.125±100ppm		GBd	1
Modulation format			PAM4		-	
Optical central wavelength	λ0	1264.5	1271	1277.5	nm	
	λ1	1284.5	1291	1297.5	nm	
	λ2	1304.5	1311	1317.5	nm	
	λ3	1324.5	1331	1337.5	nm	
Damage threshold		6.1			dBm	5
Average receive power		-9.1		5.1	dBm	6
Receive power(OMA_{outer})				3.7	dBm	
Difference in receive power between any two lanes (OMA_{outer})				4.4	dB	
Receiver reflectance				-26	dB	
Receiver sensitivity (OMAouter)	RS			-6.8	dBm	1,7,9

				–8.2 + TECQ		8,9
Stressed receiver sensitivity(OMA_{outer})				-4.3	dBm	9
Conditions of stressed receiver sensitivity test						
Stressed eye closure for PAM4(SECQ), lane under test		3.9			dB	
OMA_{outer} of each aggressor lane		-0.4			dBm	

1. Each lane.
2. Average launch power, each lane (min) is informative and not the principal indicator of signal strength.A transmitter with launch power below this value cannot be compliant; however, a value above this doesnot ensure compliance.
3. For TDECQ < 1.4 dB
4. For 1.4 dB ≤ TDECQ ≤ 3.9 dB
5. The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power.
6. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
7. Receiver sensitivity (OMAouter), each lane (max) for TECQ < 1.4 dB.
8. Receiver sensitivity (OMAouter), each lane (max) for 1.4 dB ≤ TECQ ≤ 3.9 dB.
9. Measured with conformance test signal at TP3 for the BER equal to 2.4E-4.

5.PIN DIAGRAM





6.PIN DESCRIPTION

PIN	Symbol	Description	Note
1	GND	Ground	1
2	Tx2n	Transmitter Inverted Data Input	
3	Tx2p	Transmitter Non-Inverted Data Input	
4	GND	Ground	1
5	Tx4n	Transmitter Inverted Data Input	
6	Tx4p	Transmitter Non-Inverted Data Input	
7	GND	Ground	1
8	ModSelL	Module Select	
9	ResetL	Module Reset	
10	VccRx	+3.3V Power Supply Receiver	2
11	SCL	2-wire serial interface clock	
12	SDA	2-wire serial interface data	
13	GND	Ground	1
14	Rx3p	Transmitter Non-Inverted Data Input	
15	Rx3n	Transmitter Inverted Data Input	
16	GND	Ground	1
17	Rx1p	Transmitter Non-Inverted Data Input	
18	Rx1n	Transmitter Inverted Data Input	
19	GND	Ground	1
20	GND	Ground	1
21	Rx2n	Transmitter Inverted Data Input	
22	Rx2p	Transmitter Non-Inverted Data Input	
23	GND	Ground	1
24	Rx4n	Transmitter Inverted Data Input	
25	Rx4p	Transmitter Non-Inverted Data Input	
26	GND	Ground	1
27	ModPrsL	Module Present	
28	IntL	Interrupt	
29	VccTx	+3.3V Power supply transmitter	2
30	Vcc1	+3.3V Power supply	2
31	InitMode	Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE	
32	GND	Ground	1
33	Tx3p	Transmitter Non-Inverted Data Input	
34	Tx3n	Transmitter Inverted Data Input	
35	GND	Ground	1
36	Tx1p	Transmitter Non-Inverted Data Input	
37	Tx1n	Transmitter Inverted Data Input	

38	GND	Ground	1
39	GND	Ground	1
40	Tx6n	Transmitter Inverted Data Input	
41	Tx6p	Transmitter Non-Inverted Data Input	
42	GND	Ground	1
43	Tx8n	Transmitter Inverted Data Input	
44	Tx8p	Transmitter Non-Inverted Data Input	
45	GND	Ground	1
46	Reserved	For future use	3
47	VS1	Module Vendor Specific 1	3
48	VccRx1	3.3V Power Supply	2
49	VS2	Module Vendor Specific 2	3
50	VS3	Module Vendor Specific 3	3
51	GND	Ground	1
52	Rx7p	Transmitter Non-Inverted Data Input	
53	Rx7n	Transmitter Inverted Data Input	
54	GND	Ground	1
55	Rx5p	Transmitter Non-Inverted Data Input	
56	Rx5n	Transmitter Inverted Data Input	
57	GND	Ground	1
58	GND	Ground	1
59	Rx6n	Transmitter Inverted Data Input	
60	Rx6p	Transmitter Non-Inverted Data Input	
61	GND	Ground	1
62	Rx8n	Transmitter Inverted Data Input	
63	Rx8p	Transmitter Non-Inverted Data Input	
64	GND	Ground	1
65	NC	No Connect	3
66	Reserved	For future use	3
67	VccTx1	3.3V Power Supply	2
68	Vcc2	3.3V Power Supply	2
69	Reserved	For future use	3
70	GND	Ground	1
71	Tx7p	Transmitter Non-Inverted Data Input	
72	Tx7n	Transmitter Inverted Data Input	
73	GND	Ground	1
74	Tx5p	Transmitter Non-Inverted Data Input	
75	Tx5n	Transmitter Inverted Data Input	
76	GND	Ground	1

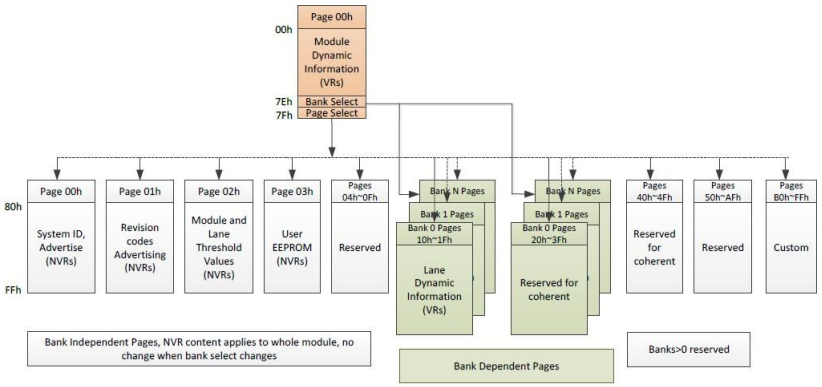
Note：

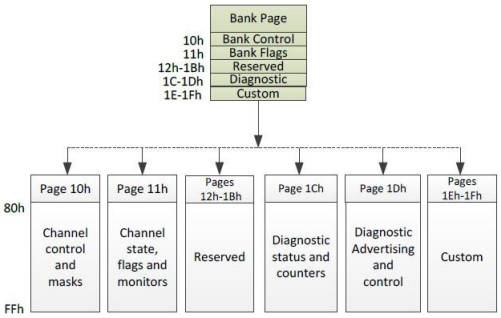
5. QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

6. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 6. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.

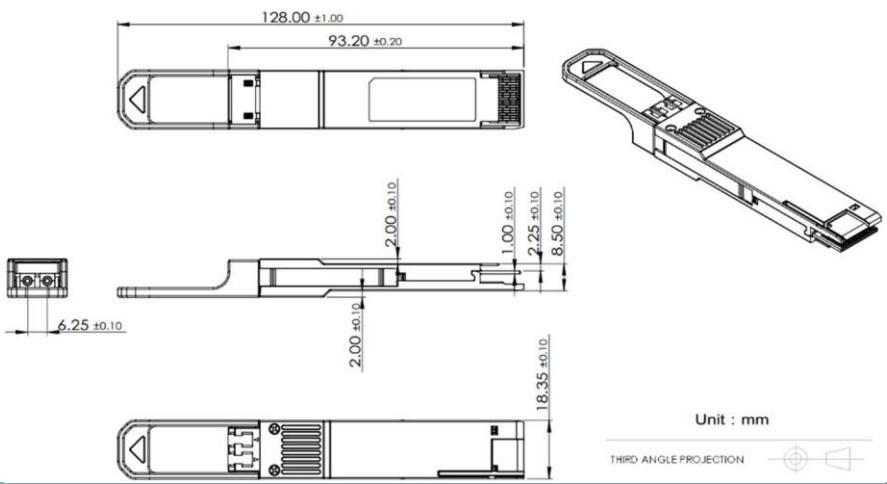
7. All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 kOhms and less than 100 pF.

7.EEPROM SECTION





8.MECHANICAL SPECIFICATION



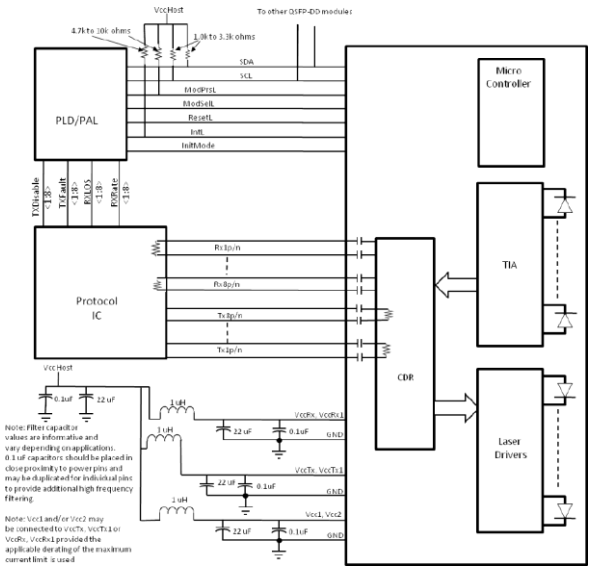
9.ESD

Product is specified as ESD threshold 1kV for high speed data pins and 2kV for all other electrical input pins, tested per MIL-STD-883, Method 3015.4 /JESD22-A114-A (HBM). However, normal ESD precautions are still required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment.

10.Laser Safety

This is a Class 1 Laser Product according to IEC 60825-1:2007. This product complies with 21 CFR 1040.10 and 1040.11 except for deviations pursuant to Laser Notice No. 50, dated (June 24, 2007).

11.RECOMMENDED CIRCUIT



12.LABEL DIAGRAM

Optowire

TD13C4L-CP

QSFP-DD 400Gb/s 1310nm 10km LR4

Class 1 Laser

MADE IN CHINA

S/N: ?????????

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